PACKAGED MEMS MICROMIRRORS FOR CRYOGENIC ENVIRONMENT

S. Waldis[1], F. Zamkotsian[2], P. Lanzoni[2], W. Noell[1] and N. de Rooij[1]
[1]Institute of Microtechnology (IMT), University of Neuchatel, Switzerland
[2]Laboratoire d'Astrophysique de Marseille (LAM), France

ABSTRACT

We are developing single-crystalline silicon micromirror arrays (MMA) for future generation infrared multiobject spectroscopy (IR MOS). Arrays of 5×5 gold-coated micromirrors were packaged and tested at below 100K. The gold-coating and the cryogenic compatibility are crucial for the application in an IR MOS. The micromirrors could be actuated before, during and after cryogenic testing. The surface deformation of the uncoated 100µm × 200µm micromirrors is below 10nm peak-to-valley (PTV), 35nm for single-side gold coated mirrors and 17nm for double-side gold coating. In cryogenic environment the PTV of the gold coated mirrors increased from 35nm to 50nm, thus still remaining in the requirements of $< \lambda/20$ for $\lambda > 1\mu m$.

1. INTRODUCTION

The observation of the formation of primary galaxies is important to understand our origins. The light coming from these faraway objects is very faint and shifted to the infrared. Multi object spectroscopy (MOS) is the central method for studying many isolated objects simultaneously, using a slit mask in the focal plane of the telescope for blocking spoiling sources and background light. These masks, performing object selection, nowadays are static perforated sheets or complex fiber-optics based systems. In the future, micro-electromechanical systems (MEMS) could provide remote controllable, reconfigurable slit mask, increasing the scientific efficiency of a MOS [1], [2].

In the framework of the studies on the future European Extremely Large Telescope (E-ELT) we are developing micromirror arrays intended to be utilized as reflective slit mask: the (astronomical) objects are selected by tilting the mirror at the corresponding sites in the focal plane and the light of these objects is sent to the spectrograph. Due to their location in the focal plane the micromirrors must be optically flat and the tilt-angle of the tilted mirrors must be uniform across the array. For achieving a high contrast between the light of the desired objects and the rejected objects the mechanical tilt-angle must be 20° or more [2]. One micromirror must be at least 100µm × 200µm in size in order to accommodate one typical astronomical object for 8m-class and up telescopes. For infrared MOS the micromirror array must work at cryogenic temperatures. Due to the latter two requirements TI DMD micromirrors are not suited as selection mask in an IR MOS.

2. DESIGN

The basic concept of the device is shown in Figure 1 (a). The MOS micromirrors are actuated electrostatically. As the device is used as object selector, it is operated in binary mode, i.e. there is an OFF and an ON state. The flat, non-actuated state of the mirrors (shown in Fig. 1 (a)) is considered as the OFF state, both mirror and electrode are grounded. The pull-in state of the mirror, precisely when the mirror is tilted as shown in Fig. 1 (d) is considered as the ON state. A single cell of the device consists of a mirror, which is suspended to a supporting frame by a flexible beam, an electrode and a spacer element that provides a constant gap between mirror and electrode. In the two-dimensional arrays the frame is designed to run along only the long side of the mirror, which makes near 100% fill-factor possible along this direction. Landing posts located on the mirror and the frame provide tilt angle control. The device consists of two different chips: the mirror chip and the electrode chip. The latter contains the spacer elements.

In order to have mirrors with a planarity better than $\lambda/20$, thick mirrors are used. With a mirror size of 100µm × 200µm, a thickness of 10µm is considered to be sufficient in order to keep the mirror flat during actuation. For infrared operation the mirrors must be gold coated. The flexion hinge type suspension is situated on the backside of the mirror. This hidden suspension beam configuration leads to a higher fill-factor than lateral suspension beams. In addition, as the suspension is covered by the mirror (except for the small gap between mirror and frame), we have no stray light coming from the bent beams, which means less degradation of the contrast. A system of landing posts (or stopper beams) on the mirror and on the frame has been developed to assure a precise and constant tilt-angle. This concept is shown in Fig. 1: Once the mirror (i.e. the landing post located on the mirror) touches the electrode, it will not stop moving but start to turn into the opposite direction around this new rotation axis. That is, the tilting angle tends to decrease once the mirror has landed. This is due to a non-zero (and opposite to the mirror tilting motion) torque around the point where the landing post is attached to the mirror. The reverse turning movement is stopped at a well-defined tilt-angle by the landing post attached to the frame adjacent the mirror. The mirror is now electrostatically clamped in a position defined by the geometry of the landing posts and the gap between electrode and mirror. Analytic modeling and FEM simulations have been used to determine the parameters of this clamping system [3]. Operation in cryogenic environment requires matching the different elements of the micromirror device in terms of their coefficients of thermal expansion (CTE) to avoid deformation or even flaking within the device when cooling down. Therefore both, mirror and electrode chip, are based on a silicon-on-insulator (SOI) wafer. The surface micromachined suspension beams on the back of the mirrors is made of polycrystalline silicon, having a CTE close to the CTE of single-crystalline silicon. The mismatch between the CTE of the gold layer on the micromirrors and the CTE of silicon can

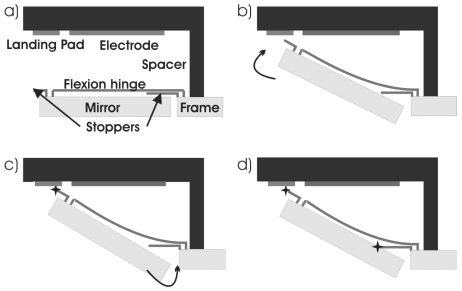


Fig. 1. Schematic view of the basic concept (a) and the electrostatic clamping mechanism used to achieve stable tilt angles: Due to the electrostatic force the mirror rotates upwards (b) until the first landing post, which is attached to the mirror, hits the electrode (c). Then the mirror starts rotating in the inverse direction until it hits the second landing post, which is attached to the mirror frame (d), and remains electrostatically fixed in this position.

hardly be avoided. However, as the silicon layer is 10µm thick and the gold layer is 100nm or less thin, the impact of the induced stress on the mirror is in an acceptable range, which will be shown below.

3. FABRICATION

The mirror and electrode chip are fabricated separately on different wafers and assembled subsequently. The mirror chip is made out of a silicon on insulator (SOI) wafer. The 10µm thick silicon on insulator layer (or, device layer) is structured into mirrors and frame by DRIE. Thermal oxidation and BPSG silicon dioxide is used to refill the trenches between mirrors and frame. Reactive ion etching is used to open the SiO2 where the suspension is attached to the mirrors and the frame. A poly-silicon layer is deposited by LPCVD and structured into suspension beams and landing posts by DRIE. DRIE is used to preserve the in-plane dimensions of the landing posts. In a final DRIE step the backside openings of the mirror and the dice free chip release trenches are etched into the 350µm handle layer. First the mirrors and then the whole chips are released in a dry HF vapor etch step [4]. The optical active side of the mirror is the backside of the device layer, which remains protected during fabrication and freed only in the very last HF vapor phase oxide etch. The micromirrors are gold coated after the backside DRIE step.

For the electrode chip an SOI substrate with a 50µm-thick device layer is used. The device layer is structured into spacers and electrodes using a selfaligned delay-mask process [5] yielding two height levels: the spacers have the initial height of the device layer thickness, while the electrodes and connecting lines are etched down to 8µm (Figs. 2-3). The wafer is diced to obtain the individual electrode chips for assembly. The electrodes of the first generation showed heights ranging from 4µm to 15µm across the wafer and the spacers a height of 48µm. Within one chip the variation of the electrode height is smaller than 100nm and the variation of the spacer height smaller than 10nm.

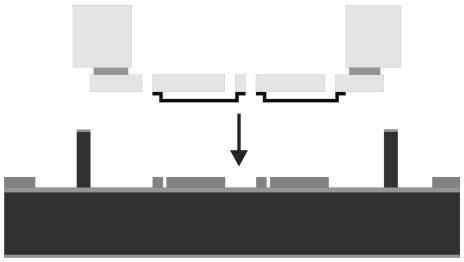


Fig. 2. Assembly step. In the last fabrication step the micromirror array is placed upside down on the integrated spacers of the electrode chip and passively aligned, as shown in Fig. 3.

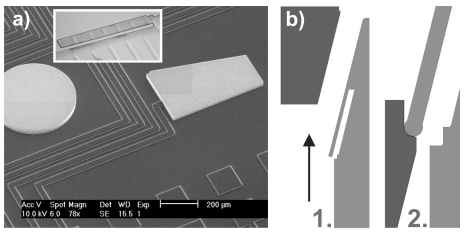


Fig. 3. SOI electrode and clip system. (a) Close-up view of a fabricated electrode chip, showing connecting lines, pads and the integrated spacers. The integrated spacers form together with the springs on the mirror chip (see inset) the guide-and-clip system used to passively align (b.1) the electrode and the mirror chip with a precision better than 5µm. Once aligned, the clip-springs snap into the indentation on the angled cuboid spacers and hold the two chips in the aligned position (b.2).

In the assembly step, the mirror chip is placed upside down on the angled cuboid spacers of the electrode (Fig. 2). The mirror chip is then pushed parallel to the angled cuboids. The angled cuboids with their counterparts on the mirror chip guide the mirror chip to the good position. Once the electrodes and mirrors are aligned, a clip system on the mirror chip snaps in and holds the mirror in the aligned position (Fig. 3). The alignment error is below 5µm. The clip system holds the device together under moderate accelerations, but for durable assembly the chip is fixed with conductive silver glue. The assembled device is packaged and wire bonded in a ceramic PGA84 housing. A printed circuit board equipped with a grid zip connector is used for easy mechanical and electrical interfacing (Fig. 4 (d)).

Arrays of 2 × 2 and 5 × 5, as well as single mirrors have been successfully fabricated (Fig. 4). Mirror sizes of 100µm × 200µm, 200µm × 100µm and 250µm × 500µm have been implemented. Flexion beams with various lengths and widths and a thickness of 0.6 µm have been realized and tested.

4. RESULTS

Optical Characterization

The surface quality of uncoated mirrors was measured in the OFF and the ON state. The 100µm × 200µm sized mirrors showed a peak-to-valley deformation of 7nm, in ON and in

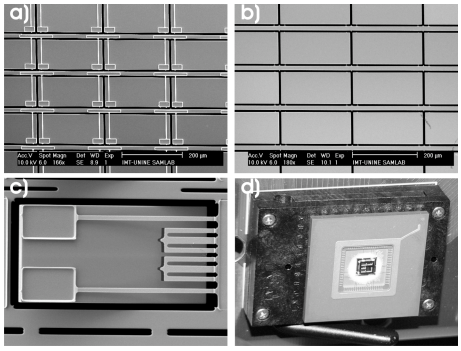
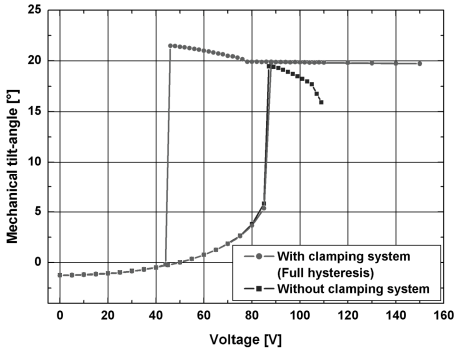


Fig. 4. Fabrication results. (a) Suspension side of a 5x5 micromirror array (b) optical side of the same array (c) single mirror showing the poly-silicon landing posts used to achieve uniform tilt angle (d) assembled and packaged micromirror device mounted on a grid zip connector allowing quick and easy interfacing.



F*ig. 5. Tilt angle versus voltage hysteresis. The mirror with the landing beam mechanism is electromechanically clamped at 20°. The angle remains stable within one arc minute over a range of 15V around the pull-in voltage.*

OFF position. As predicted, the mirrors remain flat when operated. The requirement on the flatness of the mirror is $\lambda/20$ for $\lambda > 1\mu m$, which gives 50nm. Thus our mirror quality is easily within the specifications. Larger mirrors of $250\mu m \times 500\mu m$, which may be used for larger telescopes, showed a PTV of 15nm, still satisfying the requirement on optical flatness. The local roughness is comparable to an unprocessed silicon wafer, which is around 1nm RMS. Using a reflective layer increases slightly the mirror deformation. A 50nm gold layer, with a 10nm chrome adhesion layer, is deposited on the micromirrors for good reflectivity in the near and mid-infrared range. The peak-to-valley deformation increases to about 35nm when coating only the topside of the mirror; additionally coating the backside of the mirror with the identical layers decreases the peak-to-valley deformation to 17nm. Note that the curvature of the mirror changed from concave to convex. In theory, a perfectly balanced sandwich coating would yield the initial deformation of the uncoated mirror; however in our case the backside of the mirror is partially shadowed by the suspension beams leading to a geometric asymmetry between the front- and backside coating and thus inducing this residual deformation.

Electromechanical Characterization

The mechanical tilt angle, in function of the applied voltage, has been measured for different designs of the suspension and landing post geometry. First the applied voltage is increased until the pull-in point (at 90V) or ON state (and beyond). From this point on, the voltage is decreased until the mirror snaps back to the OFF position. The tilt angle value at which the mirror snaps back, equals the maximum tilt angle the mirror has during the transition from the OFF to the ON state. The resulting tilt angle versus voltage hysteresis is plotted in Fig. 5: one mirror equipped with the landing posts and one mirror, serving as reference, without landing posts. The flat region around the pull-in point of the mirror with the landing posts proves the clamping mechanism. The landing posts hold the mirror in a stable position or more precisely, the tilt angle remains stable within one arcminute over a voltage range of 15V. This way process variations, which are translated into a variation of the tilt angle for a given voltage, can be suppressed. Thus the uniformity of the tilt angle over large arrays will merely depend on an uniform spacing between the micromirrors and the electrodes. A multicolumn system, where many columns are placed over the whole array, guaranteeing uniform spacing over large areas is currently under development.

Cryogenic Characterization

The cryogenic compatibility is crucial for the application in an infrared (IR) MOS. The operating temperature must be below 100K for near and mid IR and 30K for far IR.

Cryogenic characterization was carried out in a custom built cryogenic chamber installed on an interferometric setup. The PGA84 housing containing the sample chip is mounted via a spring loaded grid zip connector on a specially designed printed circuit board (PCB). Large copper surfaces on the PCB facilitate cooling down the system; renouncing the solder-stop layer eases outgassing of the PCB FR4 base material during evacuation of the chamber. The PCB itself is mounted via a fix-point-plane-plane attachment system to a solid aluminum block, the latter being interconnected to the cryo-generator. Thick copper wires between the PCB and the aluminum block further enhance thermal transport between the sample chip and the cryostat. Teflon-isolated electrical wires allow to interconnect up to 27 electrical connections through a Deutsch connector to the outside environment. On the outside environment the wires are connected to a custom built control electronics. Temperature sensors are connected to the aluminum block and to the grid zip connector adjacent to the sample chip. The chamber has a glass window that allows interferometric characterization of the sample chip during cryogenic testing. The micromirror device is illuminated and imagined by a CCD camera on the outside; the micromirror device is rotated such that the light of the tilted mirrors (ON state) is sent to the CCD camera.

The cryogenic chamber was cooled down until thermal equilibrium was reached. This yielded at a temperature of 86K

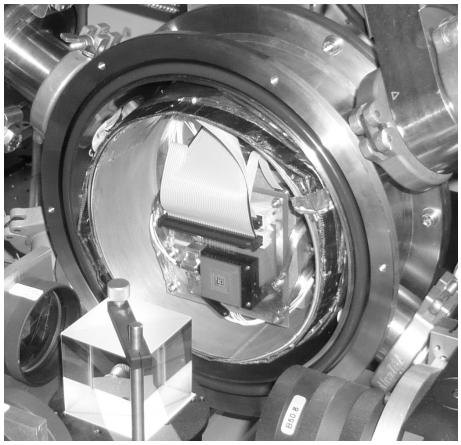


Fig. 6. Cryogenic chamber installed on an interferometric setup, allowing operational and interferometric characterization of the micromirrors at temperatures below 100K. A 5x5 micromirror array packaged in a ceramic PGA84 housing is mounted on a dedicated PCB within the chamber and interfaced via 27 leads to the outside world.

measured adjacent to the sample chip. From experience the actual temperature on the chip was estimated to be about 5K higher than on the temperature sensor adjacent. The pressure in the chamber was at 10^{-6}mbar. The peak-to-valley surface deformation of the single-side gold coated mirrors was below 50nm and thus the surface quality is still within the specifications even under these extreme conditions. The chip could successfully be actuated before, during and after cryogenic testing. Fig. 7 shows the transition from OFF to the ON state of a line of micromirrors in cryogenic environment. This proves that the micromirror device remains functional at temperatures below 100K. The actuation voltage for the mirror to snap from the OFF to the ON position was identical before and after cryogenic testing, indicating that there is no mechanical degradation of the different material interfaces. This result was confirmed by static observation in a Philips ESEM at 120K; no degradation of the critical parts of the device could be seen, the latter being: interface between electrode and mirror chip, polysilicon - single-crystalline-silicon interface and gold coating - silicon interface. Further cryogenic testing will include interferometric characterization of the surface quality and operational testing on large arrays.

5. CONCLUSION

The presented device fulfills many key parameters for the use in future Multi Object Spectrographs. It features optical flat mirrors that can be tilted by 20° with an actuation voltage below 100V. A system of landing posts which provides uniform tilt angle by electrostatically clamping of the mirrors has been demonstrated. First cryogenic experiments showed that the micromirror device is working at temperatures below

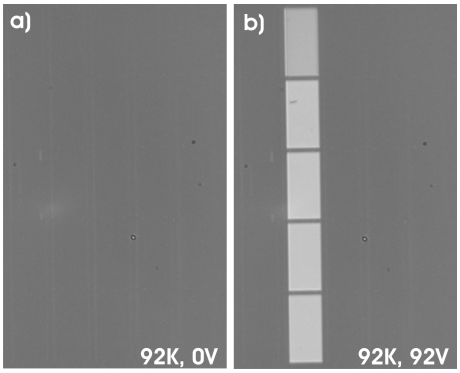


Fig. 7. Actuation test of a 5x5 micromirror array below 100K. The micromirror array in the cryogenic chamber is orientated such that the micromirrors in the tilted state send the light towards the CCD camera on the outside. First all micromirrors are grounded (a), then one line of micromirrors is actuated (b), demonstrating the operability of our micromirrors in cryogenic environment.

100K, the gold coated mirrors having a peak-to-valley deformation smaller than 50nm. Currently large arrays of up to 100 × 200 micromirrors are being fabricated.

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