Microshutter Array Development For The James Webb Space Telescope

Mary J. Li[*1], Nadine Acuna[1,2], Edward Amatucci[1], Michael Beamesderfer[1], Ray Boucarut[1], Sachi Babu[1], Sateesh Bajikar[1,2], Audrey Ewin[1], Rainer Fettig[1,3], Dave Franz[1,3], Larry Hess[1,3], Ron Hu[1,3], Murzy Jhabvala[1], Dan Kelly[1,2], Todd King[1], Gunther Kletetschka[1,6], Carl Kotechi[1], Alexander Kutyrev[1,3], Jim Loughlin[1] , Bernard A. Lynch[1,3], Harvey Moseley[1], Brent Mott[1], Bill Newell[1,4], Lance Oh[1,3], Dave Rapchun[1,3], Chris Ray[1,3], Carol Sappington[1], Eric Schulte[1,2], Scott Schwinger[1], Wayne Smith[1,4], Steve Snodgrass[1,2], Leroy Sparr[1], Rosalind Steptoe-Jackson[1], Liqin Wang[1,5], Yun (Tony) Zheng[1,2], Chris Zincke[1,2]

[1]NASA Goddard Space Flight Center, Greenbelt, MD 20771, USA
[2] QSS Group, Inc., Lanham, MD 20770, USA
[3]Raytheon Corp. ITSS, Lanham, MD 20770, USA
[4] Orbital Science Corp. ITSS, Lanham, MD 20770, USA
[5] Swales Aerospace Co., Greenbelt, MD 20705, USA
[6] The Catholic University of America, Washington D.C. 20064, USA

ABSTRACT

Micro Electromechanical System (MEMS) microshutter arrays are being developed at NASA Goddard Space Flight Center for use as a field selector of the Near Infrared Spectrograph (NIRSpec) on the James Webb Space Telescope (JWST). The microshutter arrays are designed for the spontaneous selection of a large number of objects in the sky and the transmission of light to the NIRSpec detector with high contrast. The JWST environment requires cryogenic operation at 35K. Microshutter arrays are fabricated out of silicon-on-insulator (SOI) silicon wafers. Arrays are close-packed silicon nitride membranes with a pixel size of 100x200 μm. Individual shutters are patterned with a torsion flexure permitting shutters to open 90 degrees with a minimized mechanical stress concentration. Light shields are processed for blocking light from gaps between shutters and frames. The mechanical shutter arrays are fabricated using MEMS technologies. The processing includes multi-layer metal depositions, the patterning of magnetic stripes and shutter electrodes, a reactive ion etching (RIE) to form shutters out of the nitride membrane, an anisotropic back-etch for wafer thinning, followed by a deep RIE (DRIE) back-etch to form mechanical supporting grids and release shutters from the silicon substrate. An additional metal deposition is used to form back electrodes. Shutters are actuated by a magnetic force and latched using an electrostatic force. Optical tests, addressing tests, and life tests are conducted to evaluate the performance and the reliability of microshutter arrays.

KEYWORDS: microshutter, magnetic actuation, MEMS, RIE, DRIE, micro-optics, near-infrared, space telescope

1. INTRODUCTION

The primary mission of JWST is to reveal the origins of galaxies, clusters, and large-scale structures in the universe. In order to observe galaxies at the peak of the merging and star-forming era, JWST operation requires a spectroscopic coverage in the near-infrared (NIR) wavelength region, from 0.6 to 5 μm. The NIRSpec is a Multiple Object Spectrometer (MOS)[1] allowing simultaneous observation of a large number of sources in the sky. In order to increase the observing efficiency of the spectrometer an object selector is essential to enable the simultaneous selection of multiple

[*] mary.j.li@nasa.gov, phone 301-286-9921, fax 301-286-1672; Code 553, Goddard Space Flight Center, Greenbelt, MD, 20771, USA

targets without spectral overlap on the detector. The primary requirements for the selector include: the programmable access addressing that allows more than 200 objects simultaneously selected; the high contrast with an open to closed transmission ratio of >2000; a lifetime greater than 9.4 x 10^4 cycles; and the operation in a cryogenic environment (around 35K) to assure negligible thermal emission into the spectrometer[2].

Traditional field selectors are used in a format of mechanical slits, which is not preferable in general for space flight missions due to their heavy mass and high volume. As a comparison, MEMS devices are not only light and close-packed, but also make it possible to fulfill the programmable access addressing, cover a large optical field of view, reach a high fill factor, as well as achieve a high resolution. To develop the field selector for the NIRSpec, MEMS technologies are obviously a wise choice. Several MEMS candidates were considered, including the microshutter array technology, and two micromirror array technologies[3,4]. The disadvantage of using a micromirror array as an object selector is that the mirrors are reflective devices, which diffract and scatter light. In contrast, the microshutter arrays are transmissive devices. Individual shutter cells can be actuated to a fully open position, allowing light to completely pass through the device and reach the NIRSpec detector. Microshutter devices have the potential to achieve a much higher contrast than micromirror devices. In January 2002, the microshutter array technology was selected as the MEMS candidate for the NIRSpec object selector. Since then the project has passed through several development milestones in fabrication and testing. In July 2004, the project was chosen to build the microshutter array system for flight. The delivery of the microshutter array system is scheduled in 2007, and the launch of the JWST in 2011.

The original design of microshutter arrays was in the format of 128x128 with a pixel size of 100x100 µm. The development aspects of these shutter arrays were presented in previous publications[7,8,10], covering the technical requirements, the fabrication development of 128x128 shutter arrays, the 1-D and 2-D addressing mechanisms, as well as the mechanical and optical testing. The work presented in this paper is primarily on the development of the 128 x 64 microshutter arrays with a pixel size of 100 x 200 µm. These arrays were developed for fabrication improvements, the functional testing and the reliability testing. The main focuses in the fabrication improvements included the delineation of vertical electrodes to demonstrate 2-D addressing, and the light shield development to further improve the optical contrast. Both 2-D addressing tests and life testes were conducted and demonstrated very promising results. Current work is also directed at the fabrication of the flight version of microshutter arrays. These flight arrays are required with a large format of 175 x 384 pixels and the same pixel size of 100 x 200 µm as the 64x128 arrays.

2. DESIGN AND DEVELOPMENT OF MICROSHUTTER ARRAYS

The current microshutter array design coheres of 100x200 µm (micron) unit cells. Material selection for the shutters was carried out through a series of mechanical tests and numerical analysis, as detailed in previous work[5,6]. Tests were also conducted on the mechanical response of the torsion bar to optimize their size and geometry[6]. The shutter array actuation mechanism was developed and demonstrated using prototype devices, with the goal of achieving fully programmable two-dimensional addressing and maximizing the fill-factor[7].

2.1 Unit Cell Design

Figure 1 shows a schematic of the cross-section of a unit cell, and Figure 2 gives a composite image of the front side and the backside of the device. A torsion bar connects to the frame of the device, and the shutter itself connects to the torsion bar via a small neck region. The torsion bar allows the shutters to open 90° out of plane when actuated by an external magnetic field. The shutters and torsion bars are

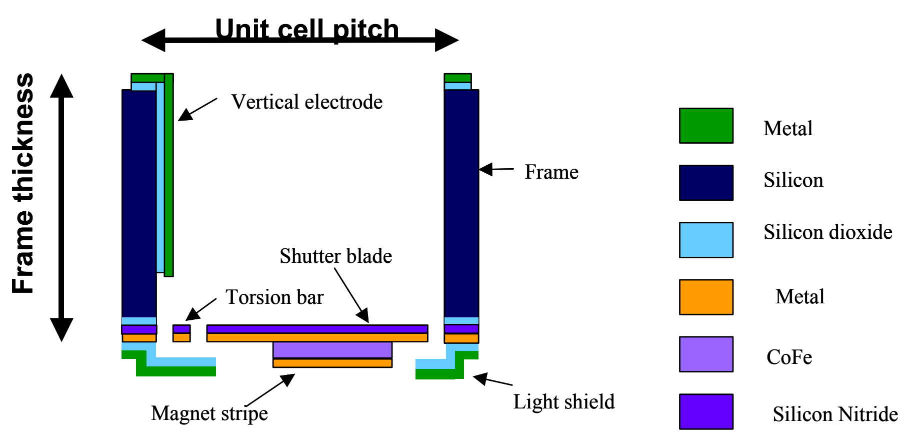


Figure 1. An unit cell of microshutter array, showing a cross-section view of a microshutter and materials used in the shutter array device.

fabricated in 5000Å-thick silicon nitride films. As shown in Figures 1 and 2, single crystal silicon grids, 100μm-deep with 8μm wall thickness, are used to support the silicon nitride film. Metal electrodes are patterned on both the front (shutter) side and back (frame) side of the shutter array. These electrodes run as strips, connecting all shutters along a given column on the front or a given row on the back. The back electrode metal is also deposited on the sidewall of the grids adjacent to the torsion bar. The front of the shutter area is coated by stripes of cobalt-Iron (90-10) alloy. This allows the shutters to be actuated by an external magnetic field. In the configuration intended for the JWST NIRSpec detector, a linear magnet aligned with the shutter rows sweeps across the underside of the array in a direction parallel to the columns. As the magnet sweeps across the array, sequential rows of shutters are rotated from their natural horizontal orientation to a vertical open position, where they approach the vertical electrodes on the sidewalls. If the electrodes are voltage-biased with a sufficient electrostatic force to overcome the mechanical restoring force of the torsion bars, the shutters will remain latched to the vertical electrodes in their open state. When the bias is insufficient or removed, the shutters will return to their horizontal closed position. The shutter actuation is demonstrated in Section 3.1.

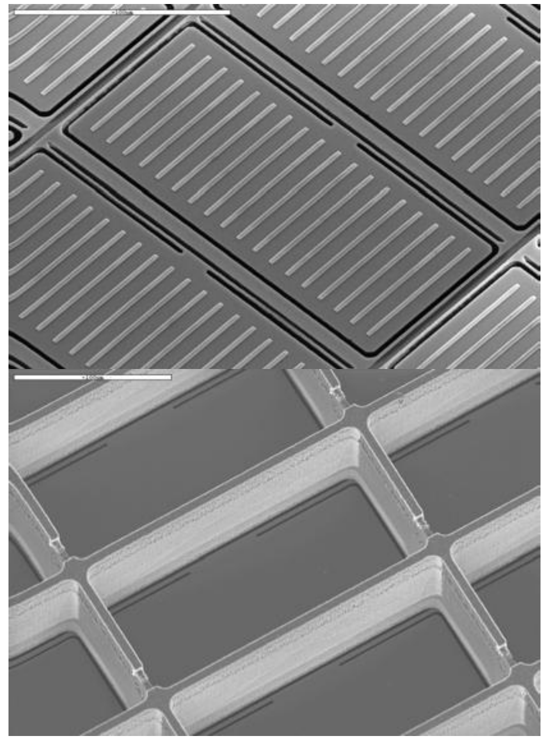


Figure 2: SEM images of the front side and backside of a 64x128 microshutter array.

2.2 Shutter Array Fabrication Development

Microshutter array fabrication is carried out through conventional semiconductor processes and MEMS technologies. Shutter arrays with 64x128 pixels are fabricated using SOI wafers. The SOI wafer consists of a 400μm silicon handle layer, a 1 μm buried silicon dioxide (oxide) layer, and a 100μm silicon device layer. A 4000Å-thick sacrificial oxide layer and 5000Å-thick nitride layer are then deposited on the wafer. The shutters arrays are all fabricated out of the device layer. Processing includes multiple metal depositions, the patterning of magnetic stripes and shutter column electrodes, the reactive ion etching (RIE) of the front side nitride to form shutters, followed by the light shield formation. The silicon handle layer is then anisotropically etched to the buried oxide layer for wafer thinning, followed by a deep RIE (DRIE) back etching down to the silicon nitride membrane. The supporting silicon grids are formed through the back etching. An additional metal deposition is conducted to form the vertical electrodes on the shutter grids. The shutters are then released from the silicon substrate by removing the sacrificial oxide layer underneath the shutters. The fabrication of each component was described in detail in previous papers[7,8]. New developments involve the light shields and the back-electrodes.

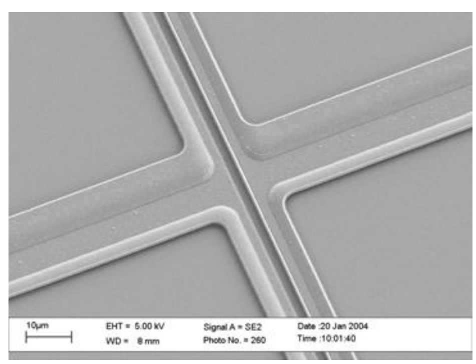


Figure 3. A SEM image shows shutters fabricated with light shields that cover the gaps and the torsion bar features.

As shown in Figures 1 and 2, there are narrow gaps between shutters and the frame. The gaps must be covered in order to block light when the shutters are in a closed position. Light shields are attached to the front electrode metal, as shown in Figure 3. Processed with a sacrificial layer, the light shields are formed as an overhang on top of the gaps. A sufficient overlap between the light shield and the shutter edge is required to minimize light leak. Figure 3 shows shutters fabricated with light shields. The light shield overhangs blocked both gaps and torsion bar features. Figure 4 shows two images of shutter arrays with and without light shields, respectively. A light source was located on the backside of the array. The array with light shields on the right demonstrated a minimal light leak, while the one without light shields on the left presented a heavy leak. The light shields greatly increased the contrast as observed in further optical tests, which will be discussed in Section 2.3.

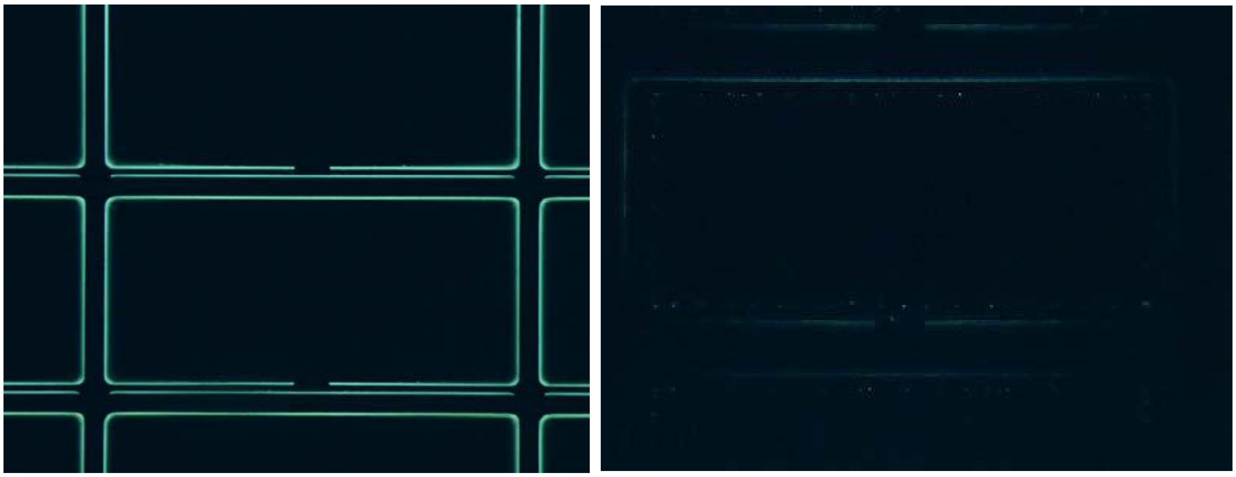


Figure 4. The array on the right with light shields demonstrated minimal light leak with a contrast ratio of 7000, while the one on the left without light shields presented a heavy leak.

As presented in a previous paper[8], both front electrodes and vertical electrodes need to be delineated in columns for the former and in rows for the latter, in order to realize the crosspoint 2-dimensional addressing of individual shutter pixels (see the Section 3.2). The delineation of the front electrodes, also called shutter electrodes, is relatively straight-forward because the involved patterning is conducted on a relatively flat surface of wafers. As illustrated in Figures 2 and 3, the shutter electrodes on the front side of an array cover all of the shutters, neck regions, torsion bars and frames. The delineation can be seen as narrow gaps between shutter columns. The delineation work for the vertical electrodes poses an unique challenge. It requires metal layers be deposited and patterned on silicon grids with 100µm-deep and several micron-wide vertical walls. Various approaches have been explored in developing a patterning technique to delineate the rows on the backside of the array[8]. The shadow masking and the mechanical dicing line to delineate neighboring rows are the two workable approaches, which were presented before, but they only work at an array level instead of a wafer level due to the difficulty of the uniformity control. The newly developed technology for vertical electrode delineation, referred to as a "shadow line", allows uniform deposition and patterning of the back electrodes at the entire wafer scale.

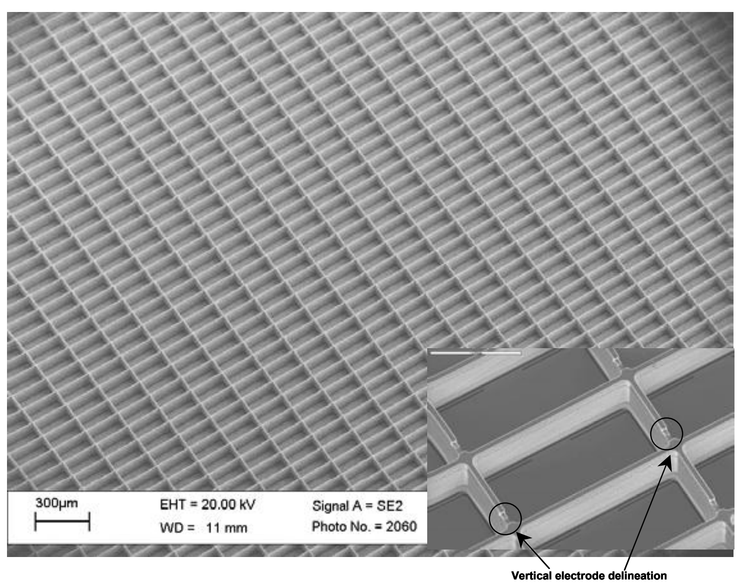


Figure 5. SEM images showing microshutter grids on the backside of a microshutter array with vertical electrodes fabricated using the Shadow Line" technology.

The shadow-line technology utilizes a double photolithographic patterning, a double DRIE etching using each pattern as a mask, and followed by an angler metal deposition for the vertical electrodes. The shadow line technology is utilized to delineate the vertical electrodes that run in rows along the long dimension of the shutters. Figure 5 shows silicon frame grids on the backside of a microshutter array with the delineated vertical electrodes. A zoom-in image in the figure indicates the locations of electrode breaks between the rows of the electrodes. The breaks, with no metal on them, then serve to isolate each row from its neighbors. Besides the narrow top of the frame grids, the metal is also deposited on one of the four vertical walls within each shutter window, which forms the important portion of vertical electrodes that contributes to the latching of shutters. As an electrical bias is applied between a vertical electrode and a shutter electrode, the shutter can be latched to the back wall, and keep the shutter in the open position (see Section 3.2).

2.3 Shutter Array Characterization and Testing

In the evaluation of microshutter arrays, two failure conditions are characterized, the failed open and the failed close. The former is defined as the light leak through a supposedly closed shutter, while the latter as the light blocked by a supposedly open shutter. The NIRSpec instrument requires the failed-close shutters < 5% and the rows with failed-open shutters <1% at the beginning of the life (BOL). It requires the failed-close shutters <20% and rows with failed-open shutters <5% at the end of the life (EOL). We have made 64x128 shutter arrays with < 1% of failed-close shutters and 0 failed-open shutter at the BOL. Accelerated life tests have being conducted on 64x128 shutter arrays with the magnetic rotisserie method and the magnetic tripole method[9].

Since the shutter electrode metal is coated on the torsion bars as well as the shutters, it is necessary to conduct mechanical tests to estimate the fatigue life of the device. Bulk metal material used for shutter electrodes fails under low cycle fatigue within hundreds or thousands of cycles when the plastic stain level is relatively high. When the shutters are fully opened, the metal on the torsion bars experiences a maximum shear strain of ~1%. However, the shutters survived 10 million cycles at a cycling rate of 20 cycles per second at room temperature without metal fatigue.

Thermal stresses from the mismatch of thermal expansion coefficients between metal films and silicon nitride, residual stresses from various depositions, as well as related tests were discussed in previous papers[8,10]. And this topic will be further discussed in future publications.

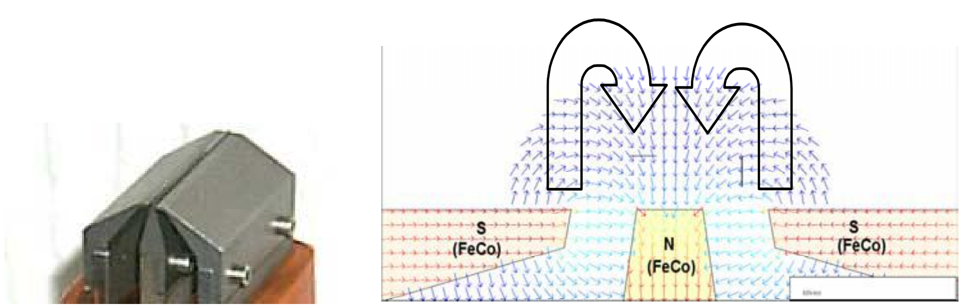
Optical tests were also conducted to evaluate 64x128 shutter arrays. Shutter arrays fabricated with light shields are able to achieve a contrast of > 7000, compared with those without light shields of ~200. The contrast is here defined as the ratio of the transmitted light where shutters are open over the one where they are close. The NIRSpec instruments requires the contrast ratio for microshutter array be >2000.

3. ACTUATION AND ADRESSING OF MICROSHUTTER ARRAYS

Both the actuation and the addressing are challenging in such close-packed microshutter arrays. A number of actuation and addressing approaches were explored in the early development stage of prototyping shutters arrays[6]. The result of the development is the mechanism of the combined magnetic actuation and electrostatic addressing. Shutters are opened by a magnetic field, latched by an electrostatic force, and selected to be open or close by addressing the electrostatic force.

3.1 Shutter Array Actuation

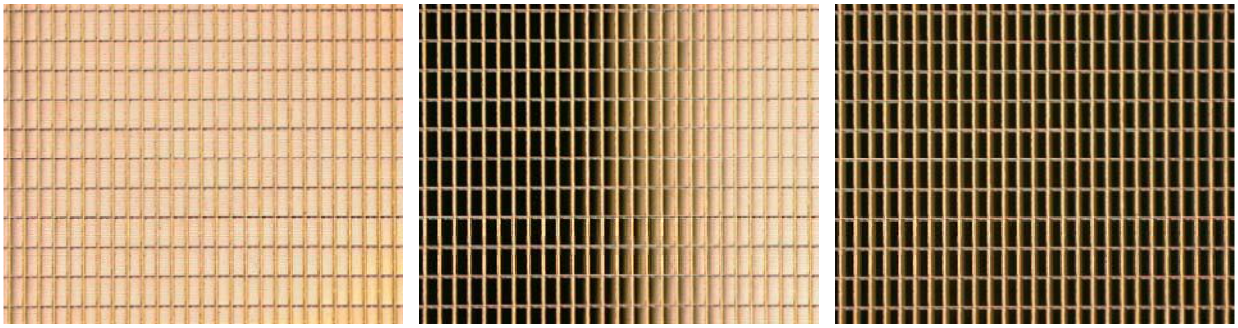
The shutters are patterned with CoFe magnetic strips as shown in Figure 2. CoFe is a ferromagnetic material with high permeability, high saturation point, and low residual magnetization. A permanent tripole magnet, as shown in Figure 6(a), is used to



(a) (b)

Figure 6. (a) A permanent tripole magnet; and (b) the magnetic field at the tip of the triple.

actuate the shutters. The magnetic field around the tip of the tripole magnet is illustrated in Figure 6(b). During the actuation, the magnet located below the shutter array (on the grid side) scans across the array. The scan opens shutters, column by column, into the shutter grids by rotating them around the torsion bars and against the back walls. The magnetic force can be controlled by the adjustment of the distance between the shutter array and the magnet.



(a) (b) (c)

Figure 7. A shutter array with CoFe magnetic stripes, (a) all shutters at a closed position, (b) partial shutters actuated, and (c) all shutters actuated.

The magnetic actuation of a 64x128 microshutter array is demonstrated in Figure 7. These images were taken using an optical microscope where a magnet located behind the array scanning from the left to the right side. In Figure 7(a), all shutters were closed when the magnet was far on the left side of the array. In Figure 7(b), shutters in the left portion of the view were open when the magnet was approaching the array from the left. Notice columns of shutters in the middle of the region were partially open because the magnetic force was relatively weak. In Figure 7(c) it shows all shutters in the region were open when the magnet was right at the center of the array behind this region. Besides the effects of the perpendicular distance between the shutter array and the magnet, the shutter actuation behavior also changes when the magnet approaches the array from the opposite direction.

3.2 Shutter Array 2-D Addressing

As shown in Figure 8, the shutter electrodes run in columns, while the back electrodes are connected in rows. Using an external crosspoint addressing scheme, all shutters can be individually selected for either open or close. Without a magnetic filed and the electrostatic force, all shutters stay closed. When the magnet opens shutters, a DC voltage is applied that generate enough electrostatic force to hold them open against the back walls that were coated with the vertical electrode metal. The DC voltage applied between shutters (front electrodes) and the back walls (vertical electrodes) is 20V on shutters and –20V on back walls. Shutters are held open when the magnet is moved away, which completes the latching process. To release a shutter, both the shutter (column) and the back wall (row) electrodes that the shutter sits in are grounded, like the first and the third shutters in the first row. Responding to the withdrawing of the electrostatic force, the shutters are released by a restoring force from their torsion bars. The shutters with either one of its electrode or both its electrodes ungrounded are held open. For example, the second shutter in the first row and the first shutter in the second row are held open with one electrode ungrounded, while the second shutter in the second row and the one in the third row are kept open with both electrodes ungrounded. The shutter releasing process can be controlled in either row by row or column by column. The voltages applied on the electrodes are a function of the restoring force on the torsion bars. The design of the geometry and the dimensions of the torsion bars is, therefore, indeed a critical factor to the latching voltages.

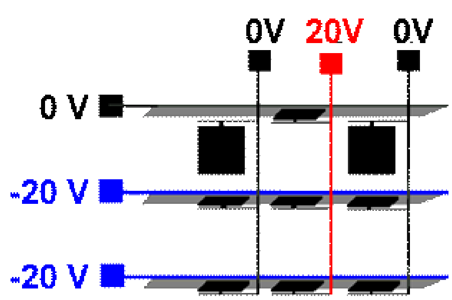
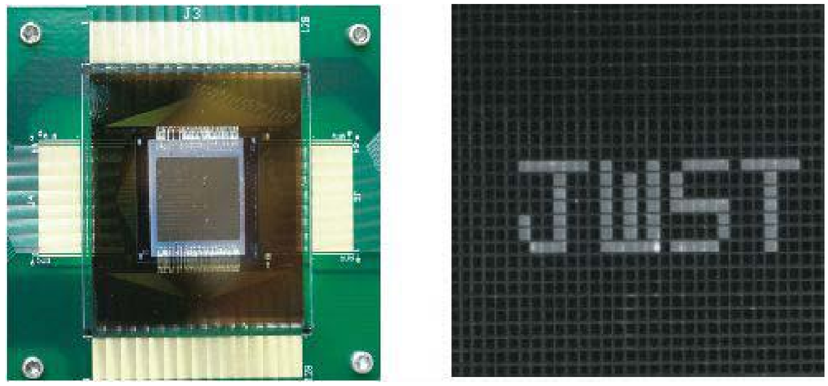


Figure 8. A schematic graph showing 2-D addressing mechanism.

In order to conduct 2-D addressing tests, a shutter array is bonded to a silicon substrate using the flip chip bonding technology. The gold bump bonding is applied to bond the shutter electrodes to the substrate to form a hybrid, shown in Figure 9(a). The vertical electrodes are connected to the substrate through a wire bonding process. The hybrid is then attached to a printed circuit (PC) board using die attaching and wire bonding that connects metal leads on the substrate to the PC board. 2-D addressing tests are performed using external electronics, either high voltage direct drive or Supertex high voltage shift registers HV583, an imaging system, and a cryogenic chamber[11]. The image in Figure 9(b) was captured from a 128x128 array during a 2-D addressing process, showing the pattern of “JWST”. The light source was located behind the array. Shutters in the letters were open and those in the background closed.



(a) (b)

Figure 9. (a) a 64x128 shutter array is flip-chip bonded on a silicon substrate and then bonded on a PC board for 2-D addressing testing. (b) An image of a shutter array showing a 2-D addressing pattern “JWST”.

4. DEVELOPMENT OF 175X384 MICROSHUTTER ARRAYS

The NIRSpec instrument requires a total area about 7.0 x 7.7 cm^2 covered by the microshutter array system. With a 100 x 200 μm^2 pixel size, 768 pixels in the dispersion direction by 350 pixels in the cross dispersion direction are needed to cover the total field of view. To meet this requirement, we will have four 175x384 microshutter arrays forming a mosaic of 2x2 array system utilizing the multi-chip module (MCM) technology. Each array will have its own silicon substrate with 2-D addressing electronics and operate independently, so that each quadrant can be replaced when it is necessary. The four quadrants will share the same magnetic actuation system and the same mechanical carrier.

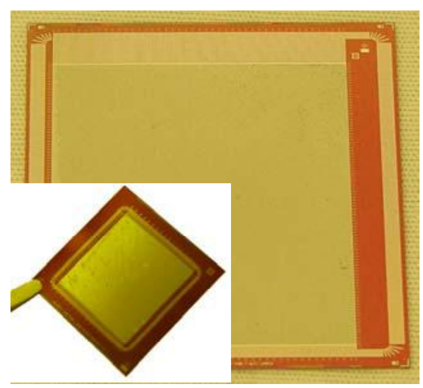


Figure 10. A 175x385 shutter array contains about 8.2 times of shutters as a 64x128 array does.

We are in the development of 175x384 arrays that are consist of 67,200 shutters. Compared to 8,192 shutters in a 64x128 array, the pixel number increased about 8.2 times. One of 175x384 arrays that we have fabricated is shown in Figure 10, as a comparison to a 64x128 array in dimensions. We are also in the development of the indium flip chip bonding process, so that 175x384 arrays can be bonded on the silicon substrates with addressing components.

5. SUMMARY AND FUTURE WORK

Microshutter arrays are being designed and fabricated as an object selector for the MOS on the JWST. Microshutter arrays are transmissive devices, minimizing light scattering to provide the high contrast needed for the near infrared spectroscopy. We have fabricated 64x128 microshutter arrays and 175x384 arrays with 100x200 μm pixel size, using combined conventional semiconductor processing and MEMS technologies. The fabrication team completed the integration of light shields to block light-leakage through gaps in the array, providing a contrast of >7000. We developed a shadow-line technology that enables us to uniformly delineate vertical electrodes on the shutter grids with the complex geometry. A series of testing on 64x128 arrays, including the 2-D addressing functional testing, the optical testing, and the reliability testing are having been conducted. The results are very promising. We are fabricating 175x384 microshutter array systems with full actuation and 2-D addressing functions. A major task remaining in the development, is making the shutter arrays working at cryogenic temperatures around 35K. We are making progress in the thermal stresses and residual stresses. The ultimate goal is providing microshutter arrays that meet the NIRSpec requirements for flight in space.

ACKNOWLEDGEMENTS

We express our appreciation to Dr. Reza Ghodssi and Mr. Wen-Hsien Chuang at the University of Maryland, College Park, for their solid support on mechanical testing, Dr. Shu-Fan Cheng at the Naval Research Lab for her persistent metal deposition work, and Mr. John Lehtonen and Ms. Katherine Mach at the Applied Physics Lab for their flip chip bonding support.

REFERENCES

[1] H. Stockman, the Next Generation Space Telescope: *visiting a time when galaxies were young,* The Association of Universities for Research in Astronomy, Inc., 1997.

[2] S. H. Moseley, R. Arendt, R. A. Boucarut, M. Jhabvala, T. King, G. Kletetschka, A.S. Kutyrev, M. Li, S Meyer, D.Rapchum, and R. F. Silververg, "Microshutter Arrays for the JWST Near Infrared Spectrograph", Proceeding of SPIE "Astronomical Telescopes and Instrumentation 2004: Space Telescopes and Astronomy", Vol.5487, 2004.

[3] J. MacKenty and M. Stiavelli, "A Multi-object Spectrometer Using Micro Mirror Arrays," in IMAGING THE UNIVERSE IN THREE DEMENSIONS: Astrophysics With Advanced Multi-Wavelength Imaging Devices, W. van Breugel and J. Bland-Hawthorn, eds., ASP Conference Series, 1999.

[4] D. J. Garcia and Nichols, "Silicon Micromirrors for the Next Generation Space Telescope," American Astronomical Society Meeting 196, pp. 2304+, May, 2000.

[5] J. Kuhn, R. Fettig, S. Moseley, A. Kutyrev, and J. Orloff, "Fracture Tests of Etched Components using a Focused Ion Beam Machine," Proceedings of SPIE4180, 2000.

[6] F. Fettig, S. Moseley, A. Kutyrev, J. Orloff, J. Kuhn, and L. Shude, "Some Aspects on the Mechanical Analysis of Micro-shutters," in Materials and Device Characterization in Micromachining II, Proceedings of SPIE 3875, 1999.

[7] S. H. Moseley, R. K. Fettig, A. S. Kutyrev, M. J. Li, D. B. Mott and B.E. Woodgate, "Status of the Development of 128x128 Microshutter Array," in MOEMS and Miniaturized Systems, Proceedings of SPIE 4178, 2000.

[8] M.J. Li, et al., "Microshutter Arrays for Near-Infrared Applications on the James Webb Space Telescope", Proceedings of SPIE 4981, 2003.

[9] T.T. King, G. Kletetschk, M.A. Jah, M.J. Li, M.D. Jhabvala, L.L. Wang, M.A. Beamesderfer, A.S. Kutyrev, R.F. Silverberg, D. Rapchun, D.S. Schwinger, G.M. Voellmer, S.H. Moseley, L.M. Sparr, "CRYOGENIC CHARACTERIZATION AND TESTING OF MAGNETICALLY-ACTUATED MICROSHUTTER ARRAYS FOR THE JAMES WEBB SPACE TELESCOPE", Workshop of Solid-State Sensor, Actuator and Microsystems, Technical Digest, p8-12, 2004.

[10] Li, M.J., I. S. Aslam, S.I.; Ewin, A.; Fettig, R.K.; Franz, D. ; Kotecki, C. , Kutyrev, A.S.; Moseley, S.H.; Monroy, C ; Mott, D.B.; Zheng, Y., "Fabrication of Microshutter Arrays for Space Application", in Microelectronic and MEMS Technologies, Proceeding of SPIE, 2001.

[11] A. S. Kutyrev, R. Arendt, S. H. Moseley, R. A. Boucarut, T. Hadjimichael, M. Jhabvala, T. King, M. Li, J. Loughlin, D. Rapchun, D. S. Schwinger and R. F. Silverberg, "Programmable Microshutter Arrays for the JWST NIRSpec: optical performance", Journal of Selected Topics in Quantum Electronics on Optical Microsystems, Vol.XX, No. XX, March 2004.